PATENT APPLICATION
Docket No. 9898-201
Client No. SS-15264-US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Hang-Yoon Lee	Conf. No.:	6427
Serial No.	10/043,724	Examiner:	Lee, Hsien Ming
Filed:	January 8, 2002	Art Unit:	2823
For:	METHOD OF FORMING SEMICONDUCTOR DEVICE HAVING CONTACT PAD ON SOURCE/DRAIN REGION IN PERIPHERAL CIRCUIT		

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P.O. Box 1450
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APPLICANT'S COMMENTS ON EXAMINER'S STATEMENT OF REASONS FOR ALLOWANCE

Applicant submits that the prior art alone or in combination does not teach a method for forming a semiconductor device on a semiconductor substrate, the method comprising: (a) forming isolation layers that define a memory cell area and a peripheral circuit area on the semiconductor substrate and isolate each area; (b) forming a first conductive type transistor in the memory cell area and a first conductive type transistor and a second conductive type transistor in the peripheral circuit area, each transistor including source/drain regions, a gate electrode having sidewall spacers, and a first etch stopping layer; (c) forming an interlayer insulating layer overlying the first and second conductive type transistors; (d) exposing the source/drain regions of the first conductive type transistor in the memory cell area and the peripheral circuit area by etching the interlayer insulating layer; (e) forming first conductive type polysilicon layers on the exposed source/drain regions of the first conductive type transistors; (f) thereafter, exposing the source/drain regions of the second conductive type transistor in the peripheral circuit area by etching the interlayer insulating layer, as recited in allowed claim 1. Applicant submits that the prior art alone or combination does not teach a method for forming a semiconductor device, comprising: (a) forming isolation layers for defining a memory cell area and a peripheral circuit area on a semiconductor substrate and isolating each area; (b) forming a first conductive type transistor in the memory cell area and a first conductive type transistor and a second conductive type transistor in the peripheral circuit area by forming source/drain regions and gate electrodes

having sidewall spacers, and first etch stopping layers in the memory cell area and the peripheral circuit area of the semiconductor substrate; (c) forming conductive epitaxial layers, which extend from the source/drain regions onto the isolation layers, on the respective source/drain regions; (d) forming an interlayer insulating layer overlying the transistors and the conductive epitaxial layers; (e) forming plugs by patterning the interlayer insulating layer, and forming openings in the interlayer insulating layer to expose the source/drain regions of the transistors in the memory cell area and the peripheral circuit area, and filling the openings with metal; and (f) concurrently forming metal contact pads in the memory cell area and the peripheral circuit area. (g) forming a second conductive type polysilicon layer on the exposed source/drain regions of the second conductive type transistor; and (h) concurrently forming contact pads on the source/drain regions in the memory cell area and the source/drain regions in the peripheral circuit area, as recited in allowed claim 9. Applicant submits that the prior art alone or combination does not teach a method of forming a semiconductor device having metal contact pads on source/drain regions of transistors in a peripheral circuit area for writing and reading data in memory cells on a semiconductor substrate, the method comprising: (a) forming first and second gate electrodes having sidewall spacers and etch stopping layers in the peripheral circuit area; (b) forming an interlayer insulating layer overlying the first and second gate electrodes; (c) forming first and second conductive type transistors by forming an opening in portions of the interlayer insulating layer on an active area including the first and second gate electrodes, implanting first and second conductive type impurities into the opening, and forming source/drain regions; (d) forming a metal layer in the opening; and (e) forming metal contact pads by node-separating the metal layer, as recited in allowed claim 16. Applicant submits that the prior art alone or in combination does not teach a method of forming a semiconductor device including a memory cell area having a plurality of memory cells and a peripheral circuit area for writing and reading data in the memory cell area of a semiconductor substrate, the method comprising: (a) forming isolation layers for defining a memory cell area and a peripheral circuit area on the semiconductor substrate and isolating each area; (b) forming a first conductive type transistor in the memory cell area and a first conductive type transistor and a second conductive type transistor in the peripheral circuit area by forming source/drain regions and gate electrodes having sidewall spacers, and first etch stopping layers in the memory cell area and the peripheral circuit area of the semiconductor substrate; (c) forming a first insulating layer overlying the transistors; (d) forming plugs by patterning the insulating layer, forming openings in the first insulating layer to expose the source/drain regions of the transistors in the memory cell area and the peripheral circuit area, and filling the openings with a conductive material; (e) forming contact pads on the source/drain regions in the memory cell area and the source/drain regions in the peripheral circuit

area, concurrently by etching the first insulating layer and the plugs and then node-separating the plugs; (f) forming a second etch stopping layer on the contact pads; (g) forming a second insulating layer on the contact pads with the second etch stopping layer; and (h) forming a contact plug on at least one contact pad, as recited in allowed claim 21. Applicant submits that the prior art alone or in combination does not teach A method for forming a semiconductor device on a semiconductor substrate, the method comprising: a. forming isolation layers that define a memory cell area and a peripheral circuit area on the semiconductor substrate and isolate each area; b. forming a first conductive type transistor in the memory cell area and a first conductive type transistor and a second conductive type transistor in the peripheral circuit area, each transistor including source/drain regions, a gate electrode having sidewall spacers, and an etch stopping layer; c. forming an interlayer insulating layer overlying the first and second conductive type transistors; d. etching the interlayer insulating layer to expose the source/drain regions of the first conductive type transistor in the memory cell area and the peripheral circuit area by; e. forming first conductive type polysilicon layers on the exposed source/drain regions of the first conductive type transistors; f. thereafter, etching the interlayer insulating layer to expose the source/drain regions of the second conductive type transistor in the peripheral circuit area; and g. forming a second conductive type polysilicon layer on the exposed source/drain regions of the second conductive type transistor; and h. etching back the interlayer insulating layer to form contact pads concurrently on the source/drain regions in the memory cell area and on the source/drain regions in the peripheral circuit area, as recited in allowed claim 24.

The remaining claims further distinguish over the prior art.

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Respectfully submitted,

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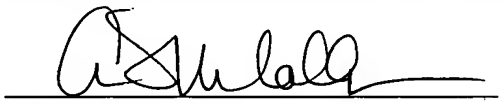

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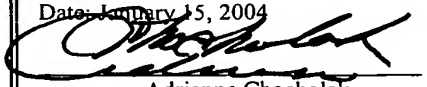

Adrienne Chocholak

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TRANSMITTAL LETTER

Enclosed for filing in the above-referenced application are the following:

- ☒ Applicant's Comments on Examiner's Statement of Reasons for Allowance
- ☒ Publication and Issue Fee
- ☒ In connection with issuance of a patent:
  - ☐ Supplemental Declaration ☒ PTO Form 85B
- ☒ PTO Form 2038 authorizing credit card payment of $1630.00, issue fee ($130.00) and publication fee ($300.00) is enclosed.
- ☒ Any deficiency or overpayment should be charged or credited to deposit account number 13-1703.

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Respectfully submitted,

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